

Compal Confidential

Model Name :PILP1  
File Name : LA-6921P

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## LA-6921 Edge Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH + Whistler 128bit with BACO

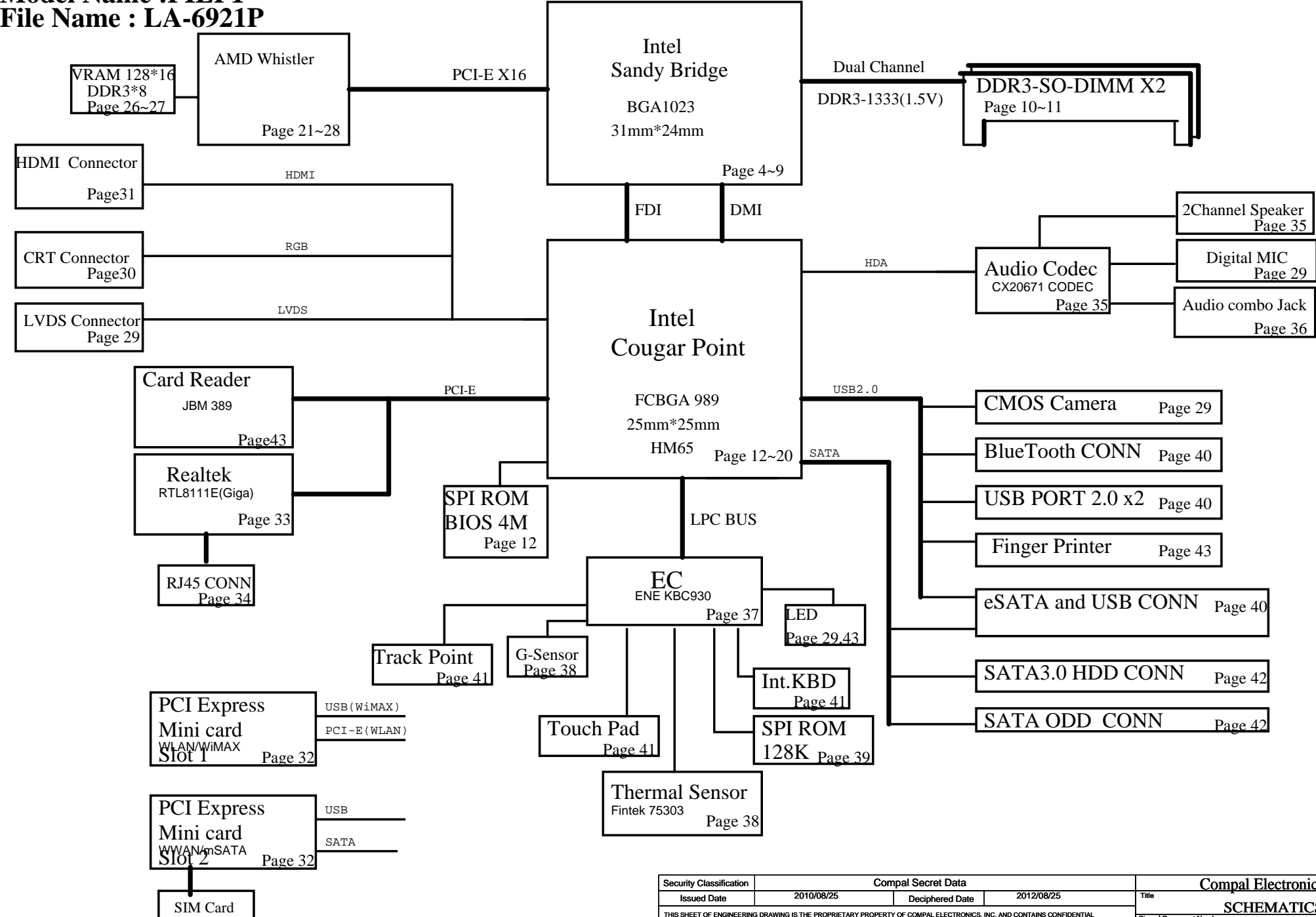
2010-11-30

REV:1.0

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Voltage Rails				
power plane				
State				
	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.0VS +VGFX_CORE +CPU_CORE +0.75VS +1.5VS_DISVGA +1.0VS +NVVDD +3VS_DISVGA +1.8VS_DISVGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
Full ON		HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF

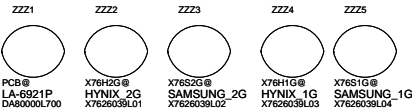
BOARD ID Table	
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB_COMBO
		1	USB_PORT
	UHCI1	2	NO USE
		3	NO USE
	UHCI2	4	WWAN
		5	CAMERA
EHCI2	UHCI3	6	HM65 not support
		7	HM65 not support
	UHCI4	8	WLAN
		9	USB_CHARGER
	UHCI5	10	NO USE
		11	NO USE
	UHCI6	12	FINGER-PRINTER
		13	BLUETOOTH

Structure	Function
CPU1@	CPU type
PX@	PX4.0 SKU
UMA@	UMA SKU
3G@	3G Sim card
X76H1G@	VRAM
PCB@	M/B

Vcc	3.3V +/- 5%				
R613	100K +/- 5%				
Board ID	R682	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0K +/- 5%	0 V	0 V	0 V	SDV1
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	SVT

PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA
1	1	0	PX4.0



EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

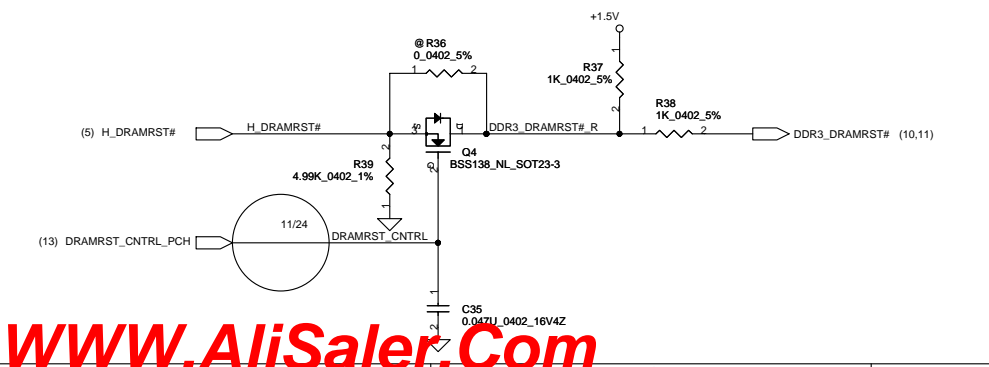
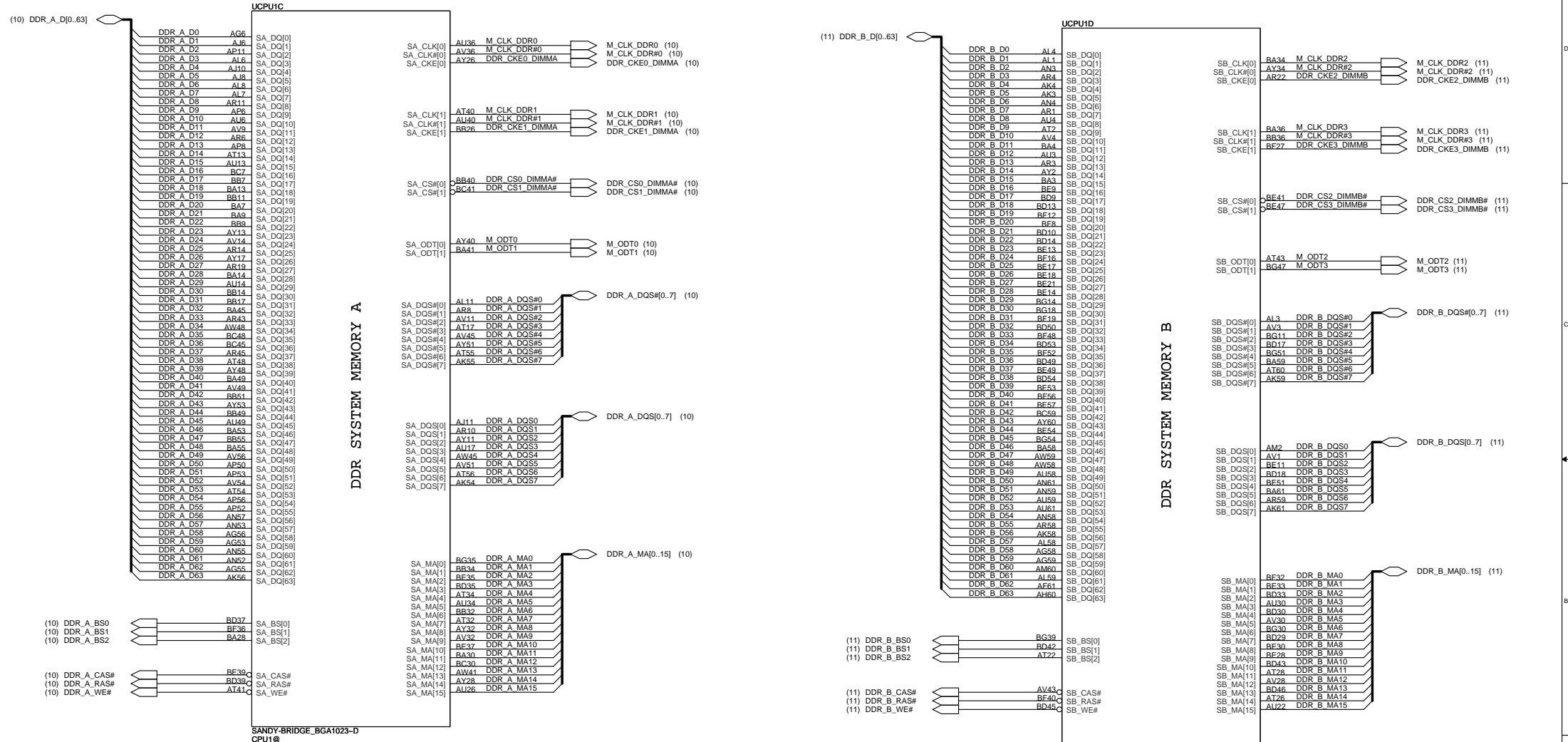
Device	Address
PCH	1001 0110 b
Thermal sensor(U30)	1001 101x b
GPU(U9)	1000_0010 b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 000xb
DDR DIMM2	1010 010xb
EEPROM(U32)	1010 100xb







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VID[0]	VID[1]		2011	2012
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0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

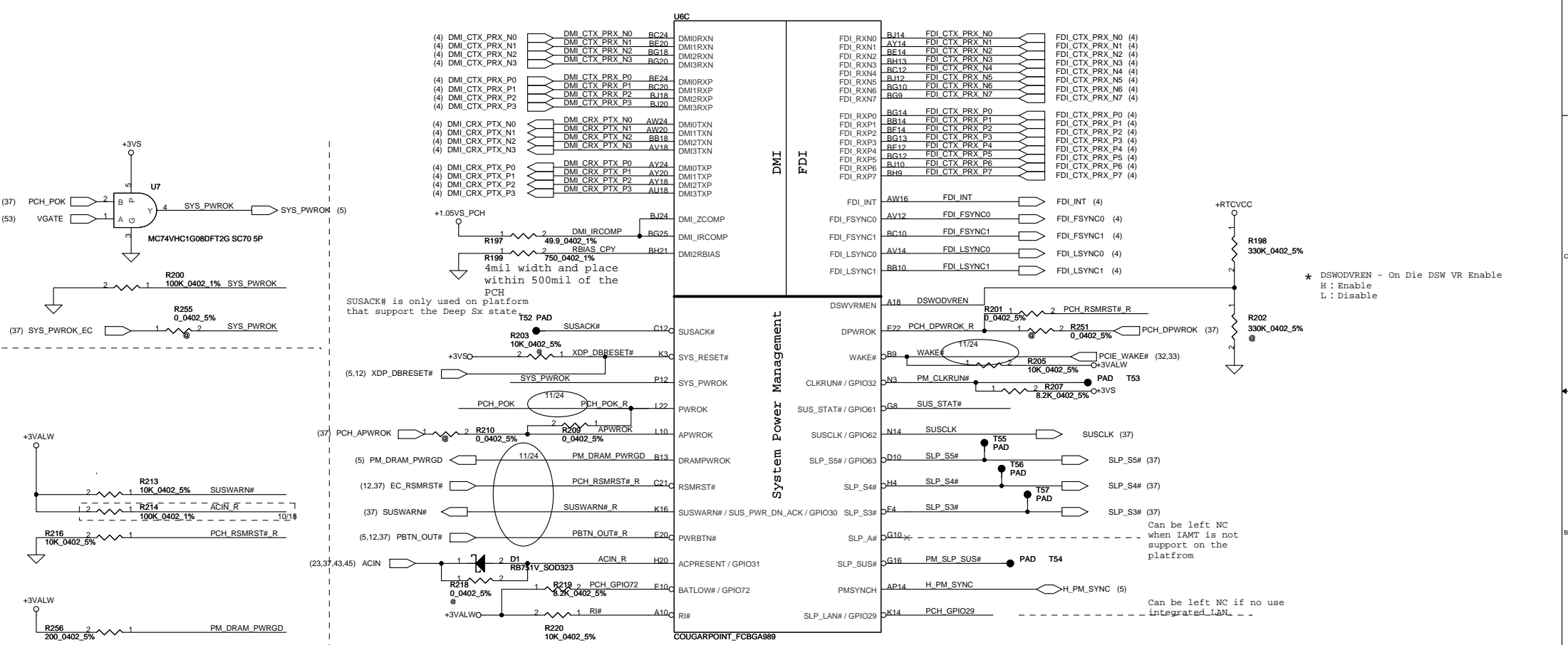
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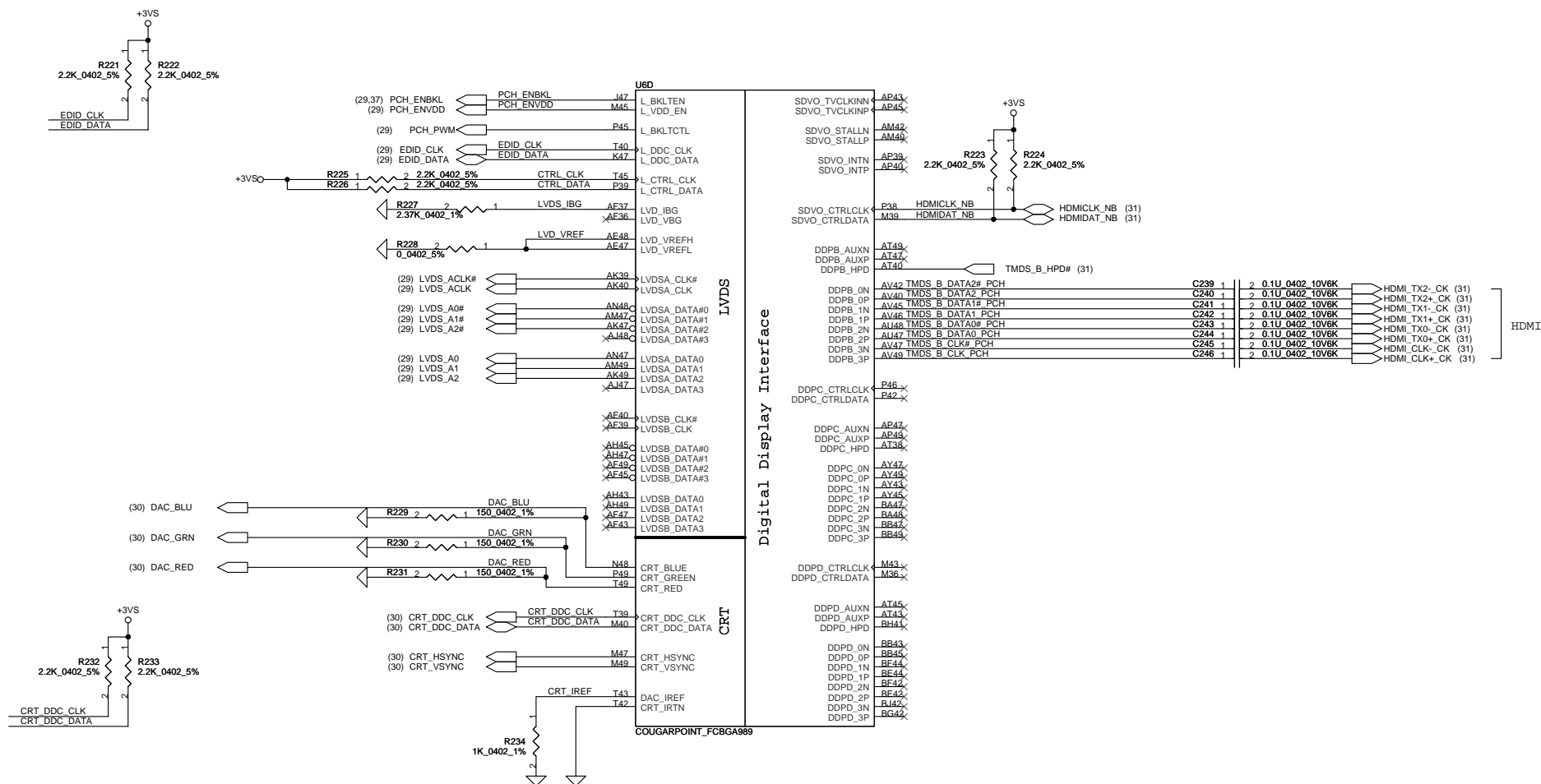






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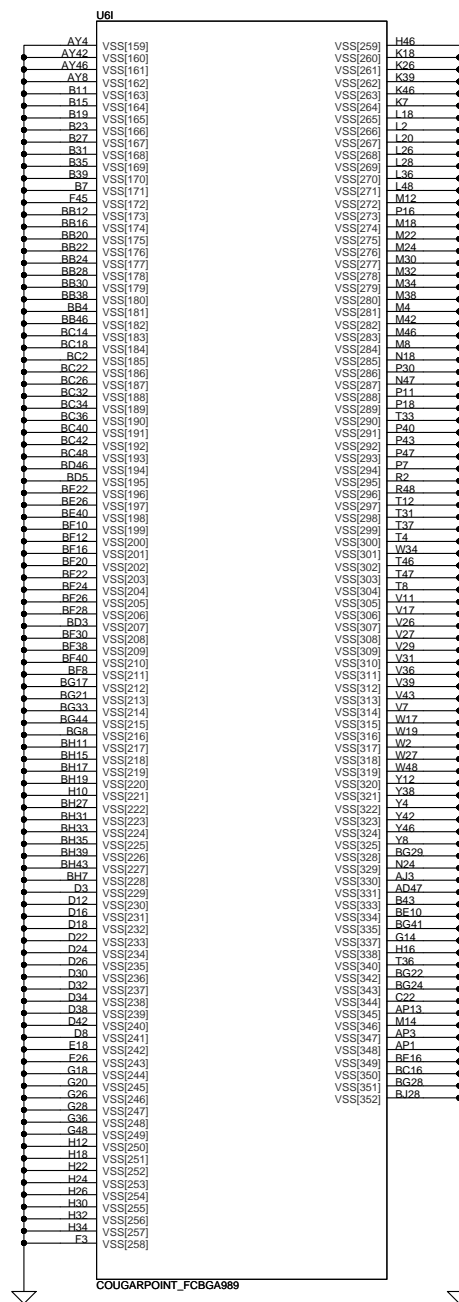
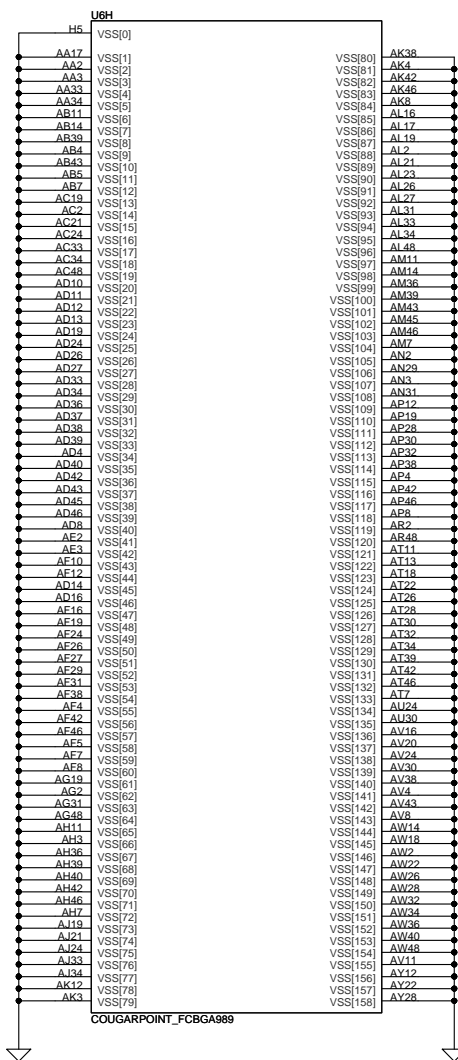








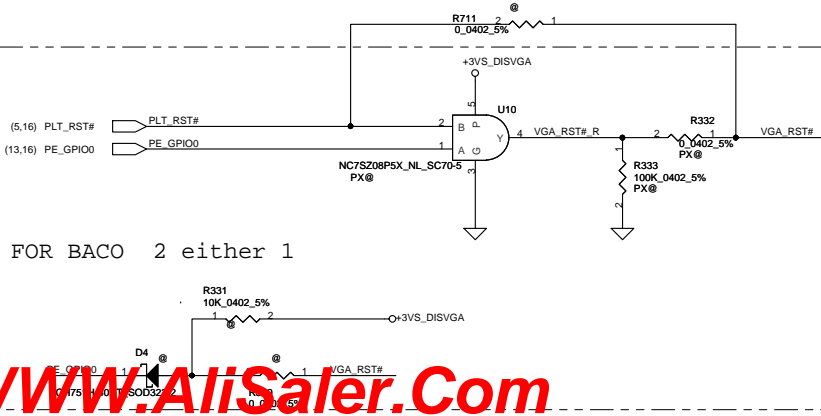
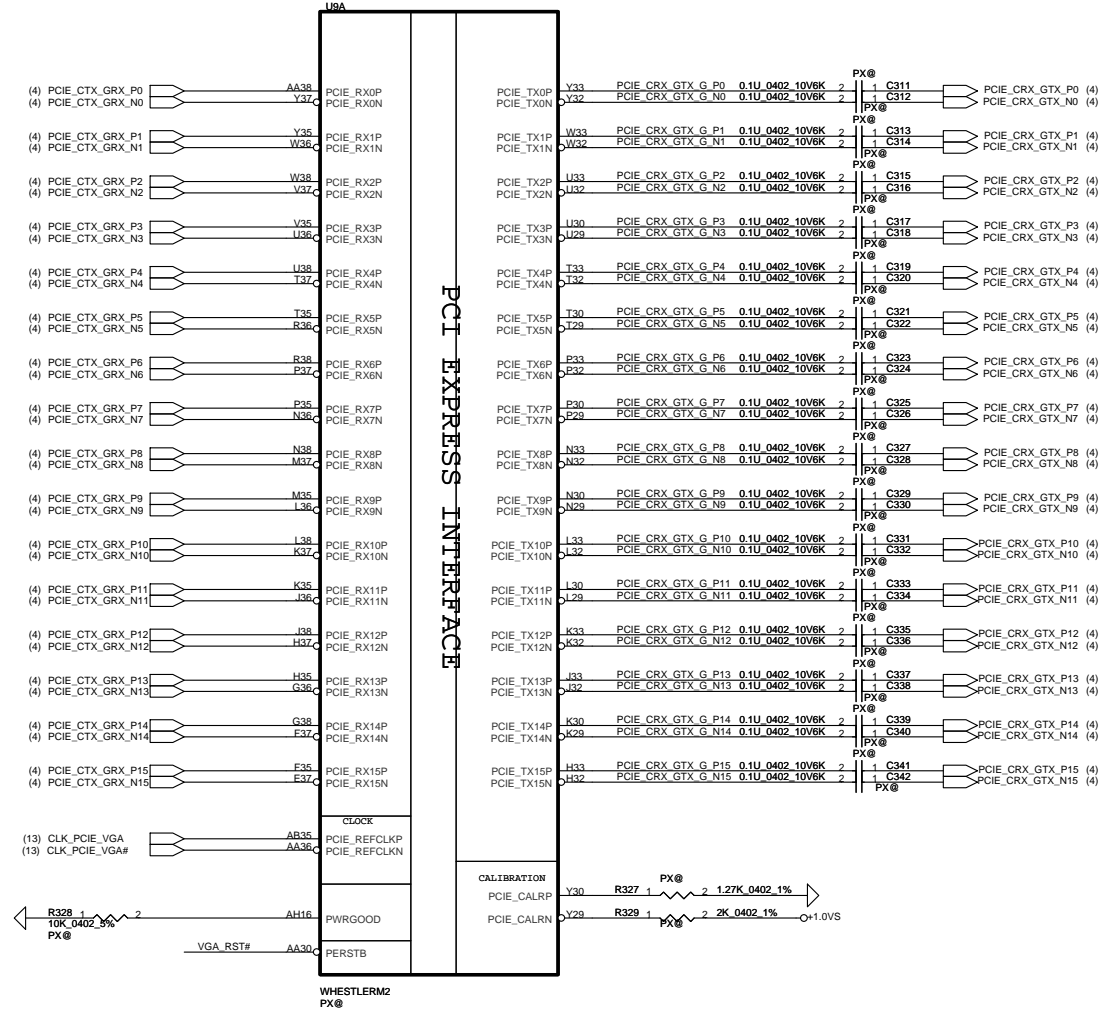
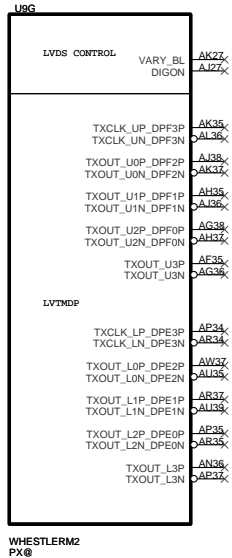




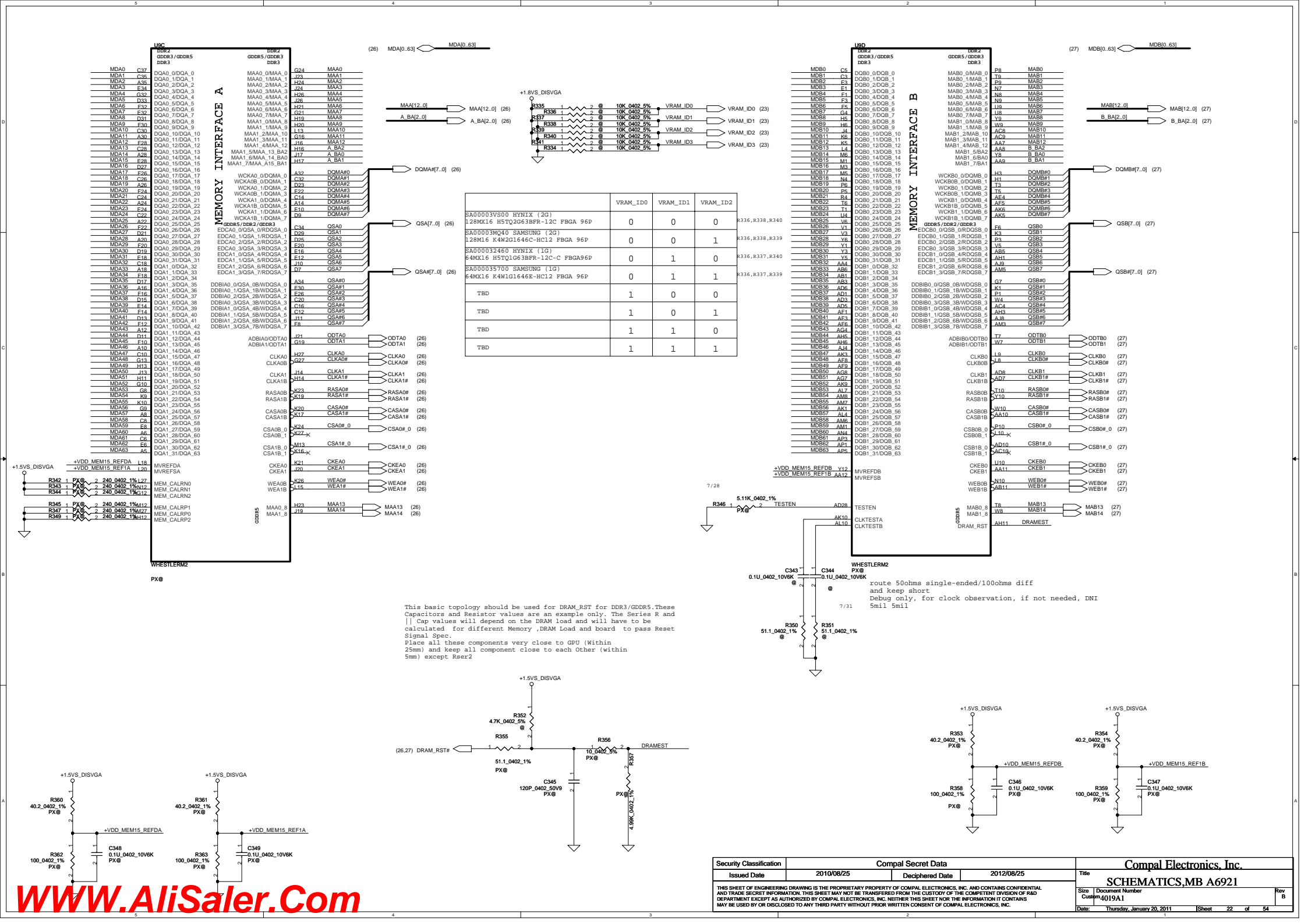
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# PEG Interface

## LVDS Interface



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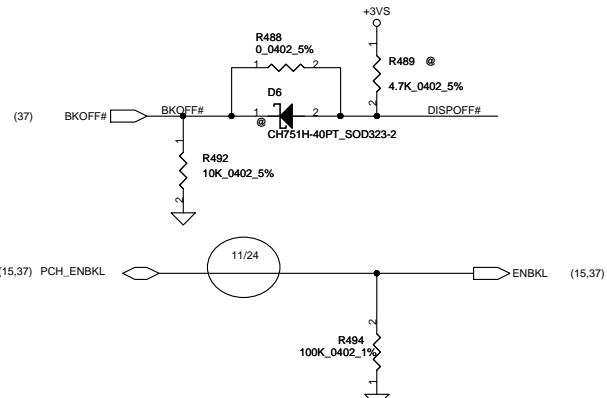
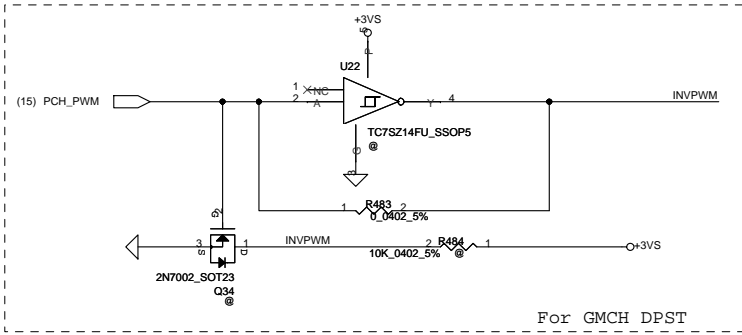
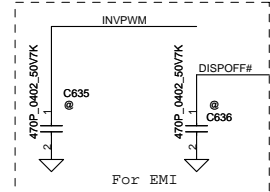
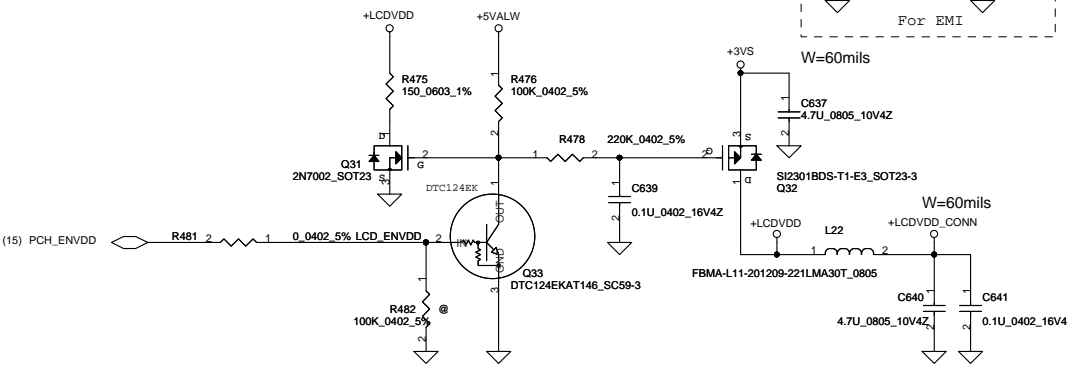




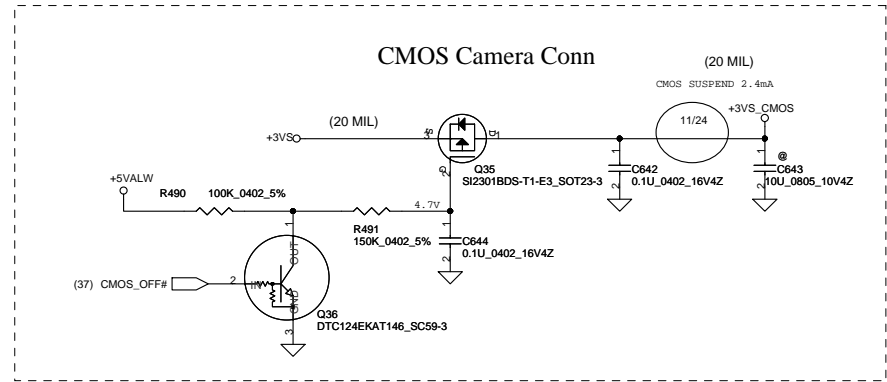
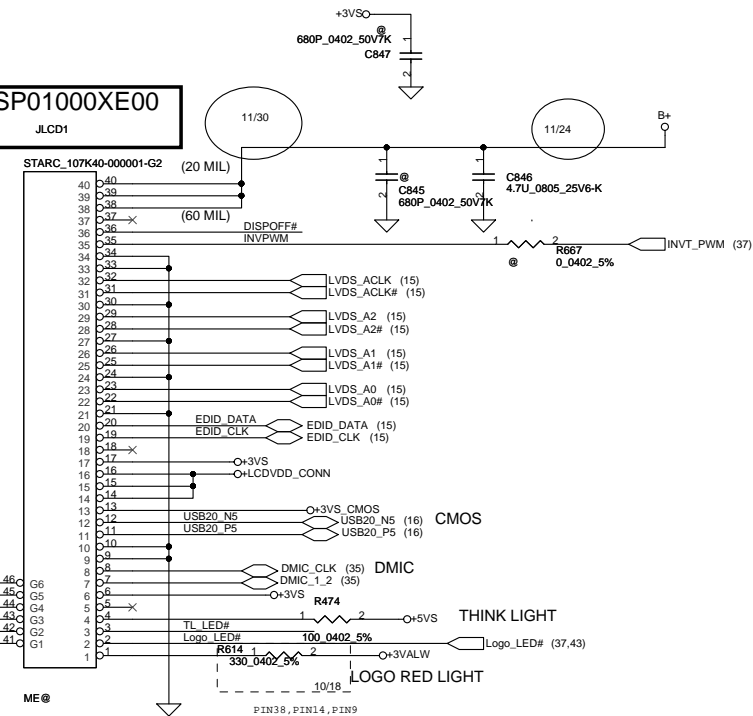




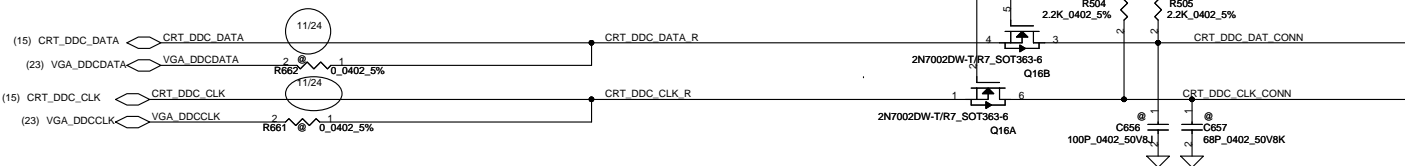
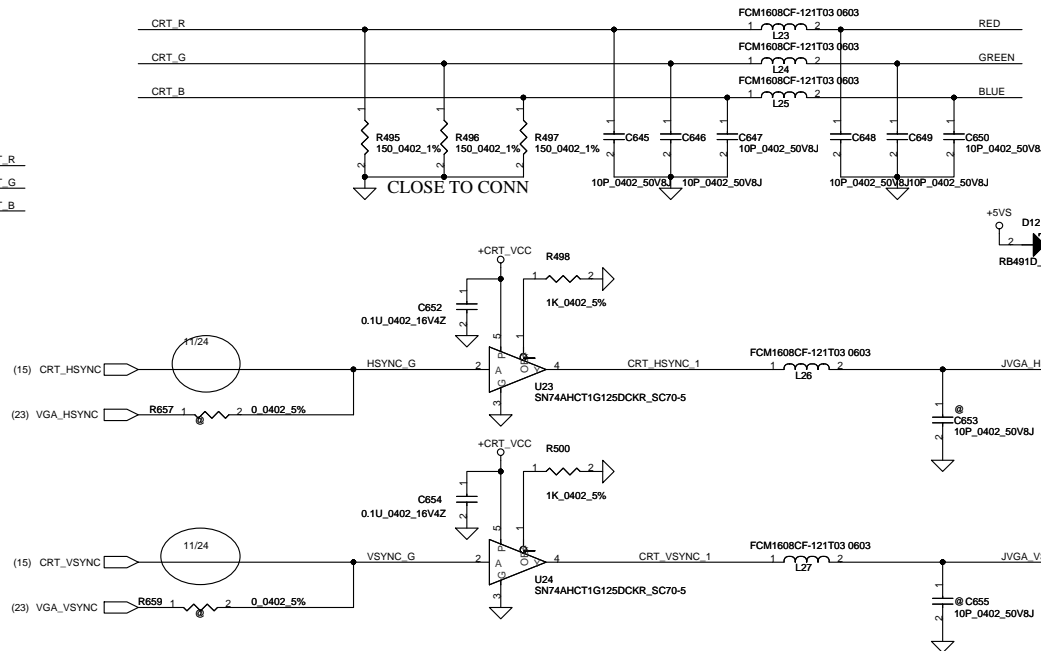
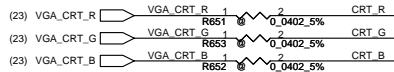
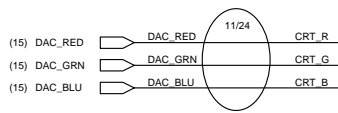
# LCD POWER CIRCUIT



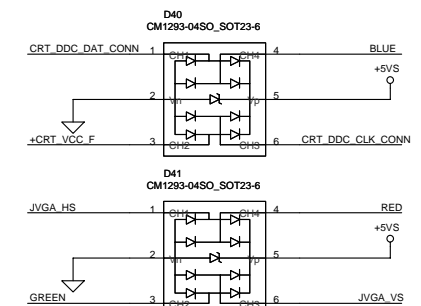
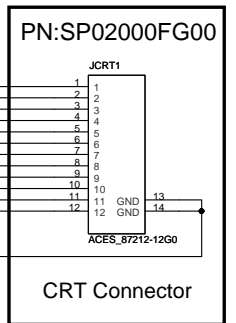
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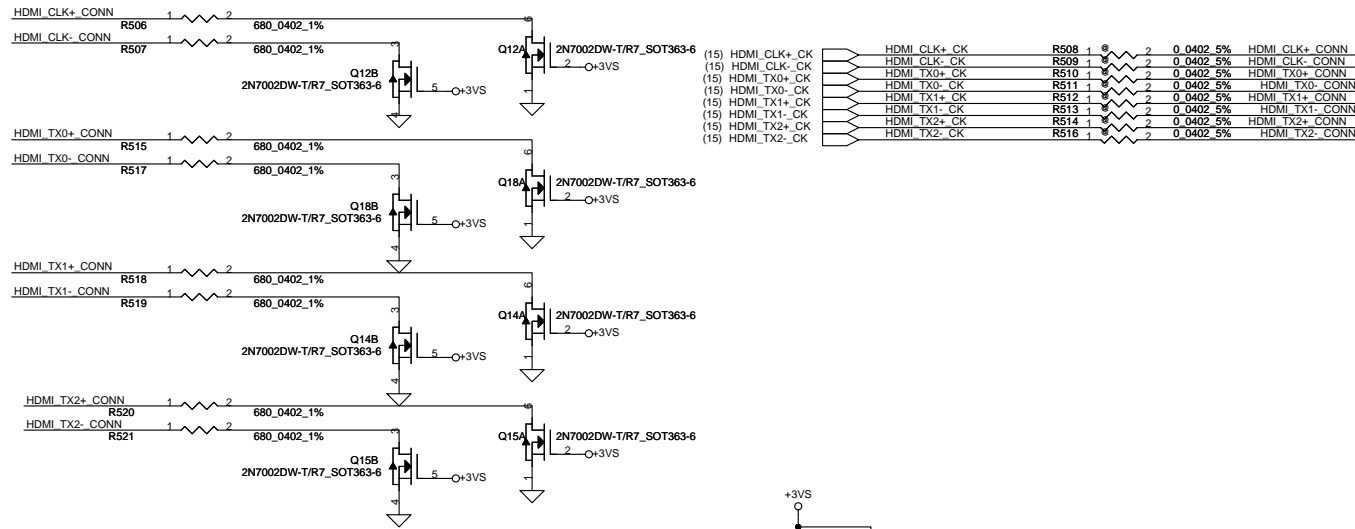


CRT Connector

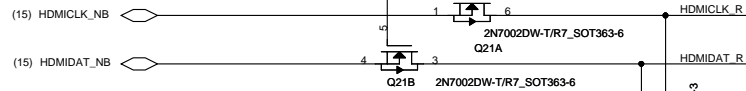


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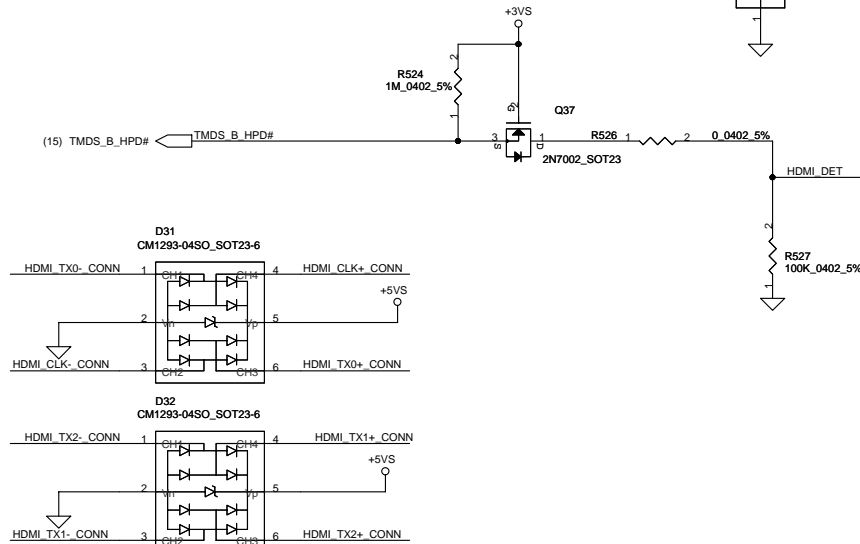
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Pull up R for PCH SIDE

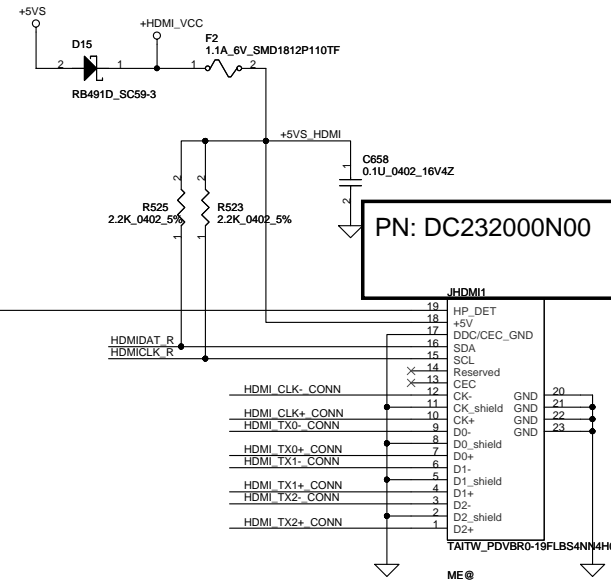
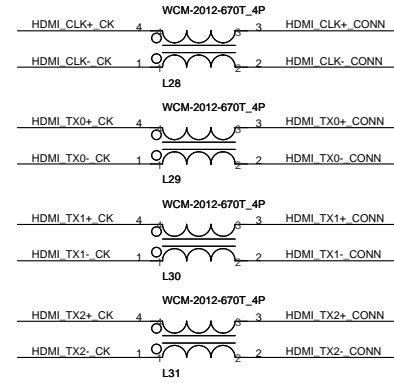


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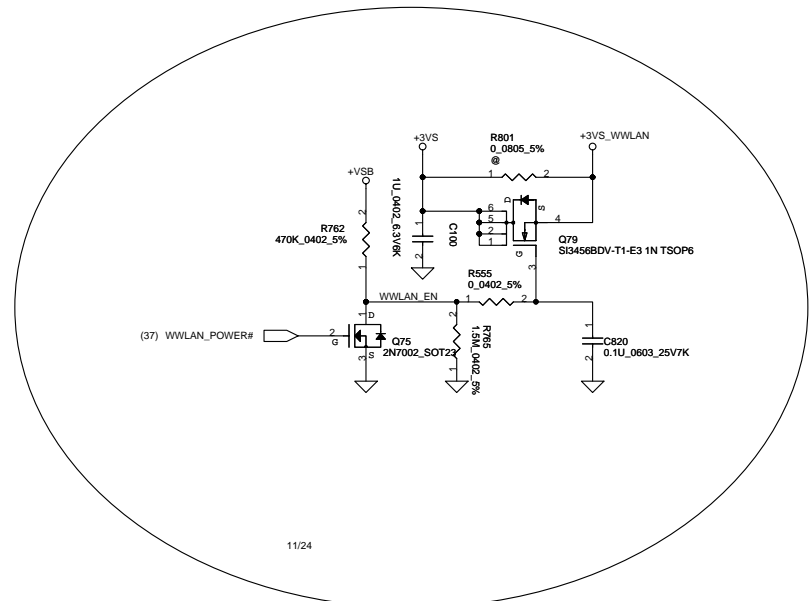
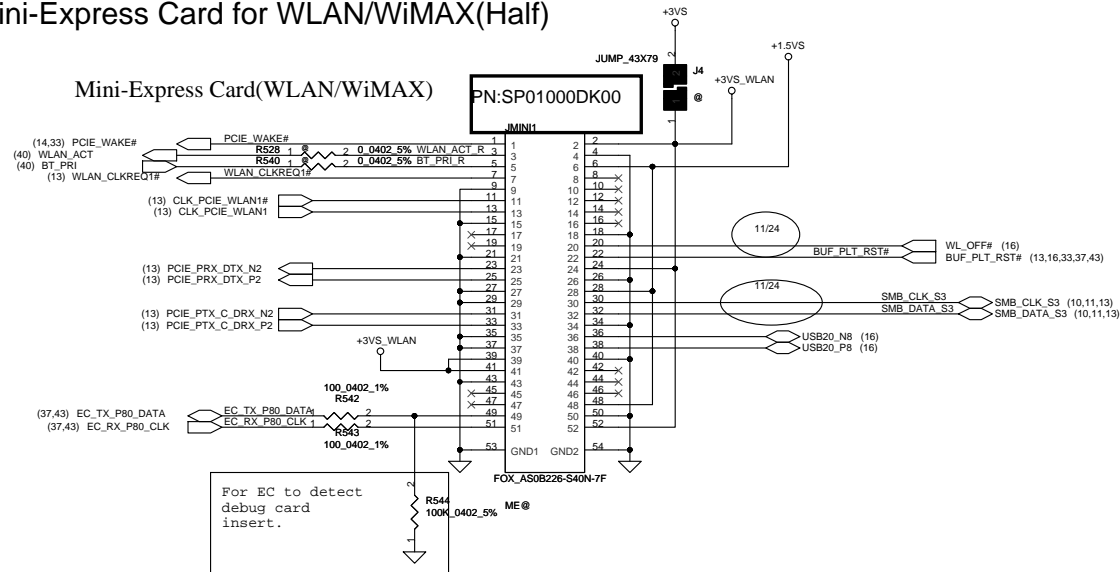
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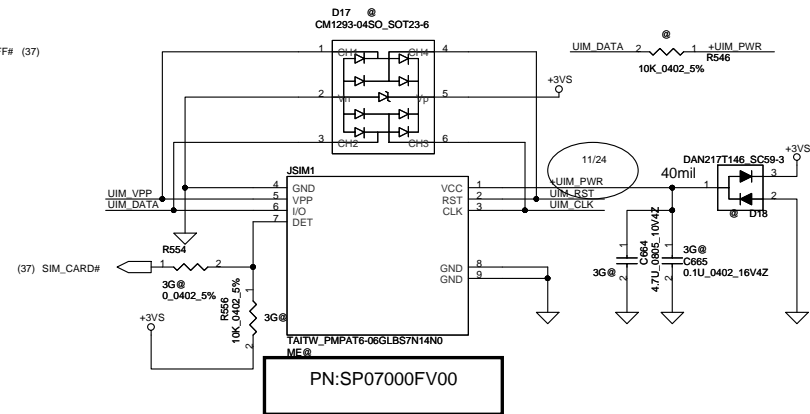
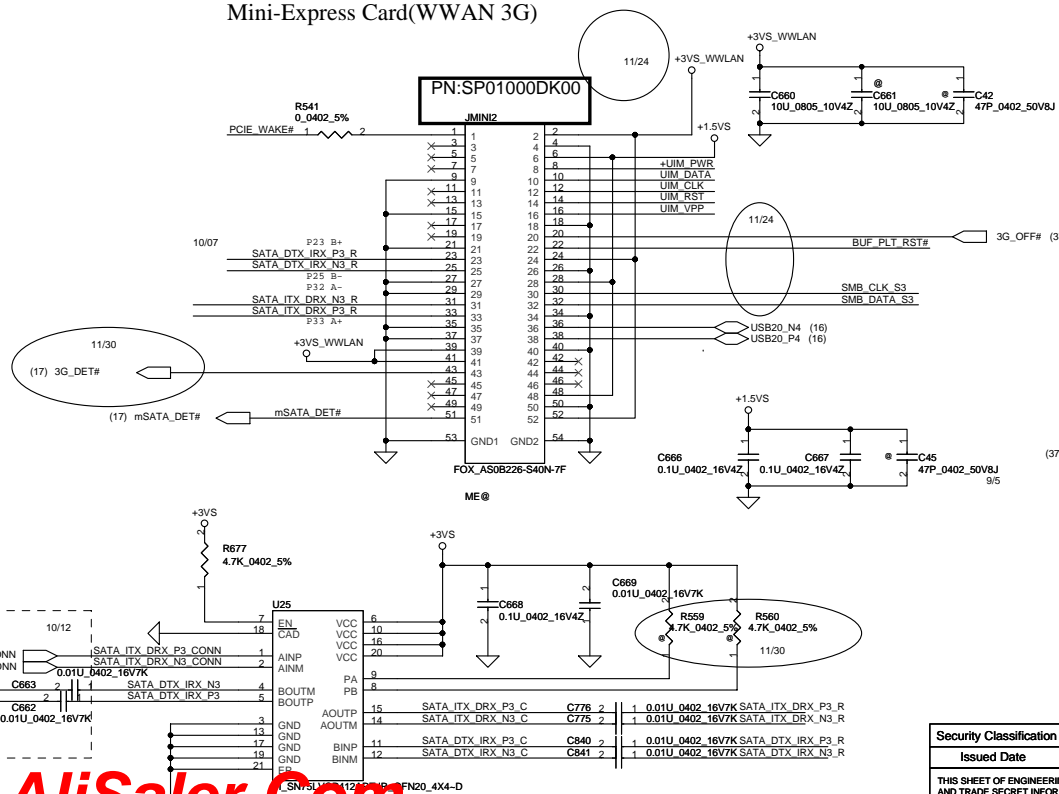
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# Mini-Express Card for WLAN/WiMAX(Half)



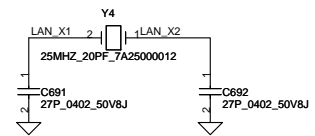
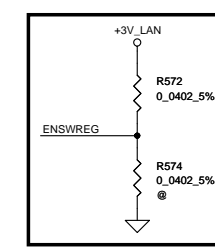
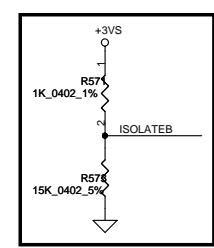
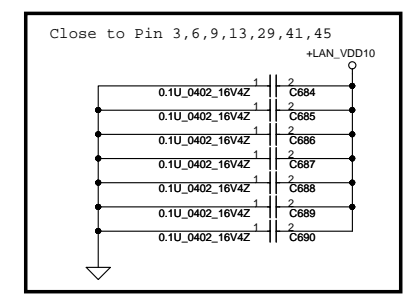
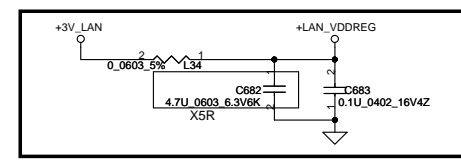
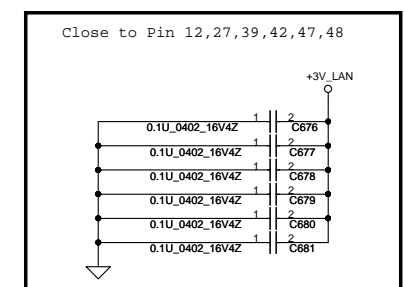
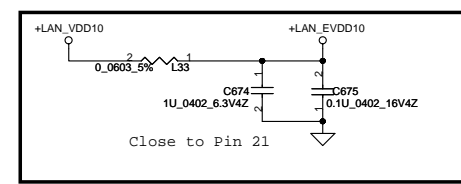
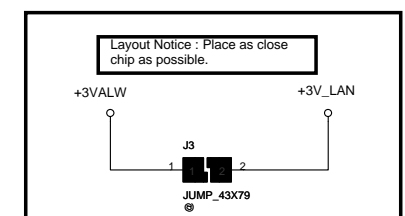
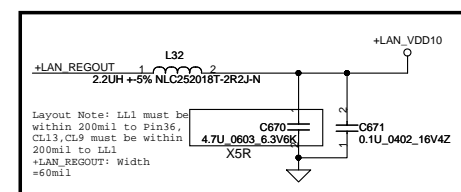
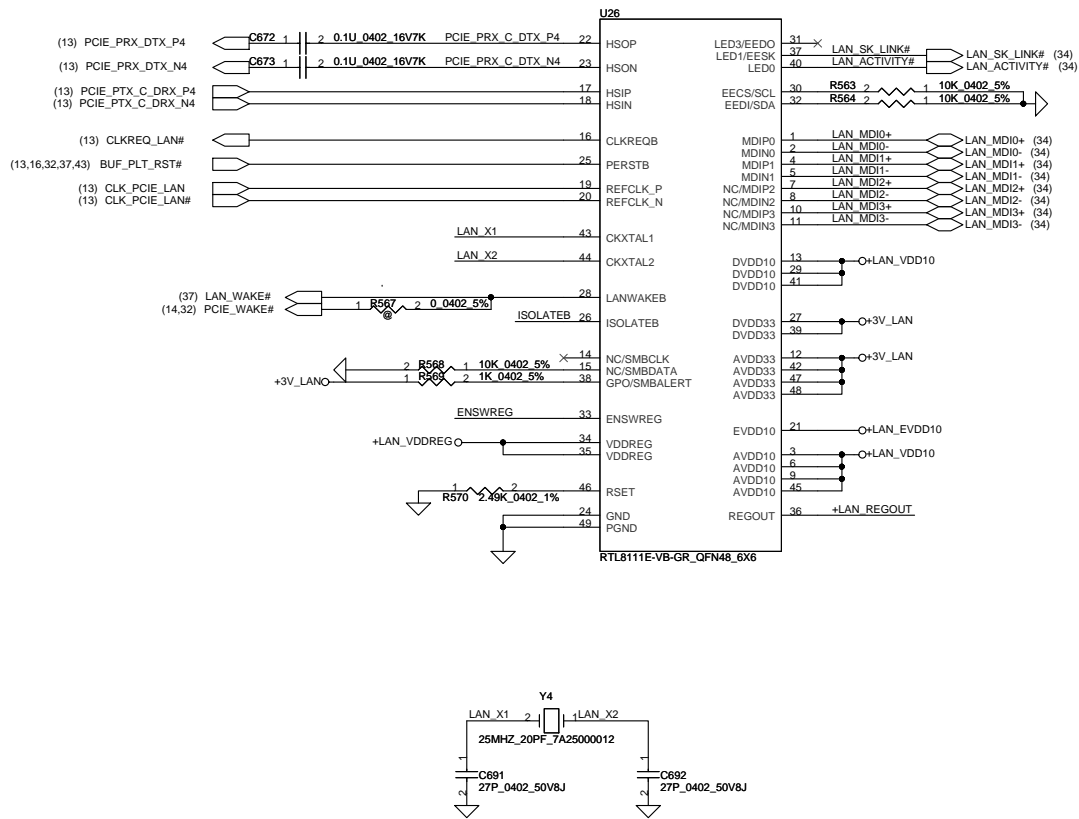
# Mini-Express Card for WWAN/mSATA(Full)

## Mini-Express Card(WWAN 3G)



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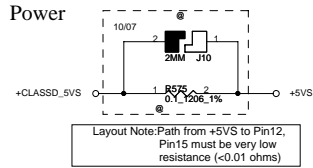




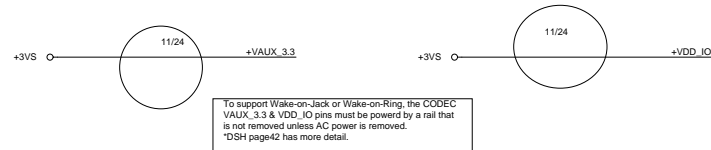
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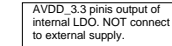
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



Layout Note: Path from +5VS to Pin12, Pin15 must be very low resistance (<0.01 ohms)

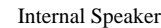
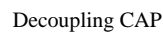


To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX\_3.3 & VDD\_IO pins must be powered by a rail that is not removed unless AC power is removed.  
\*DSH page42 has more detail.



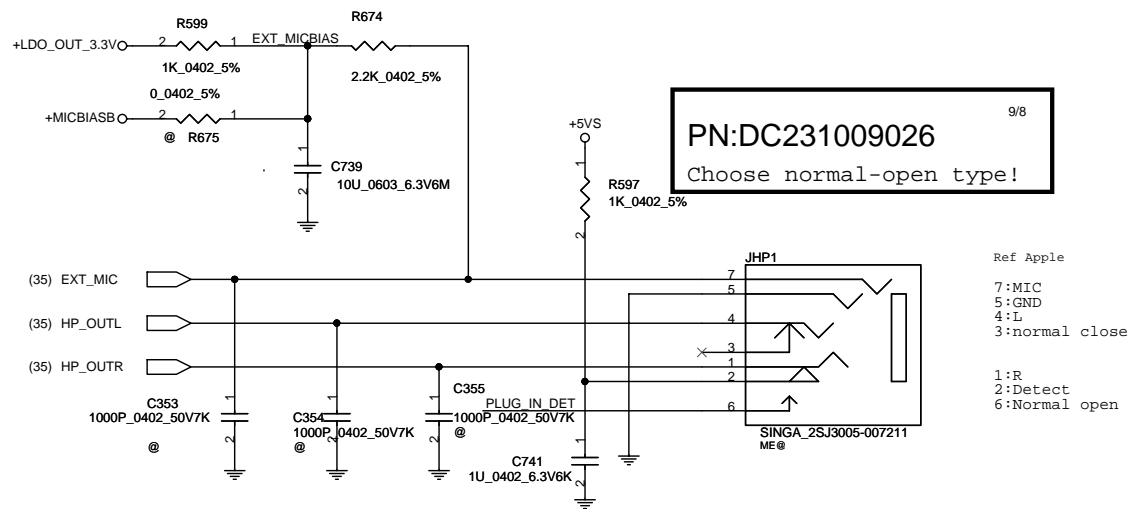
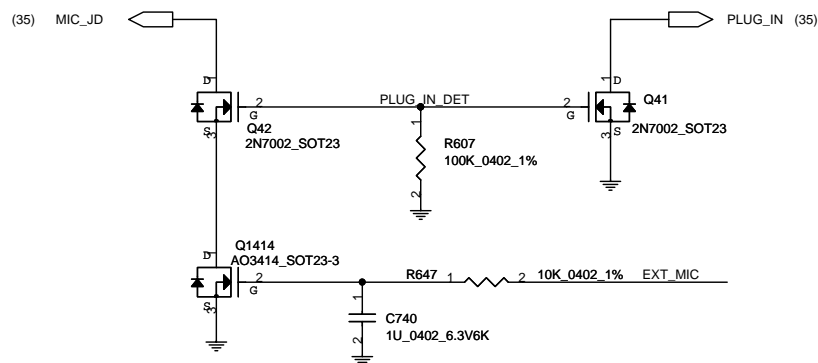
Sense resistors must be connected same power that is used for

Changed from 5.1ohm to 15ohm  
for "zi zi" noise.



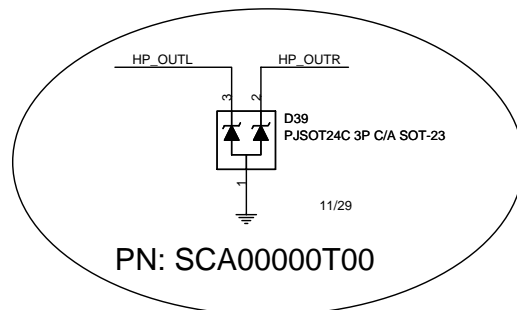
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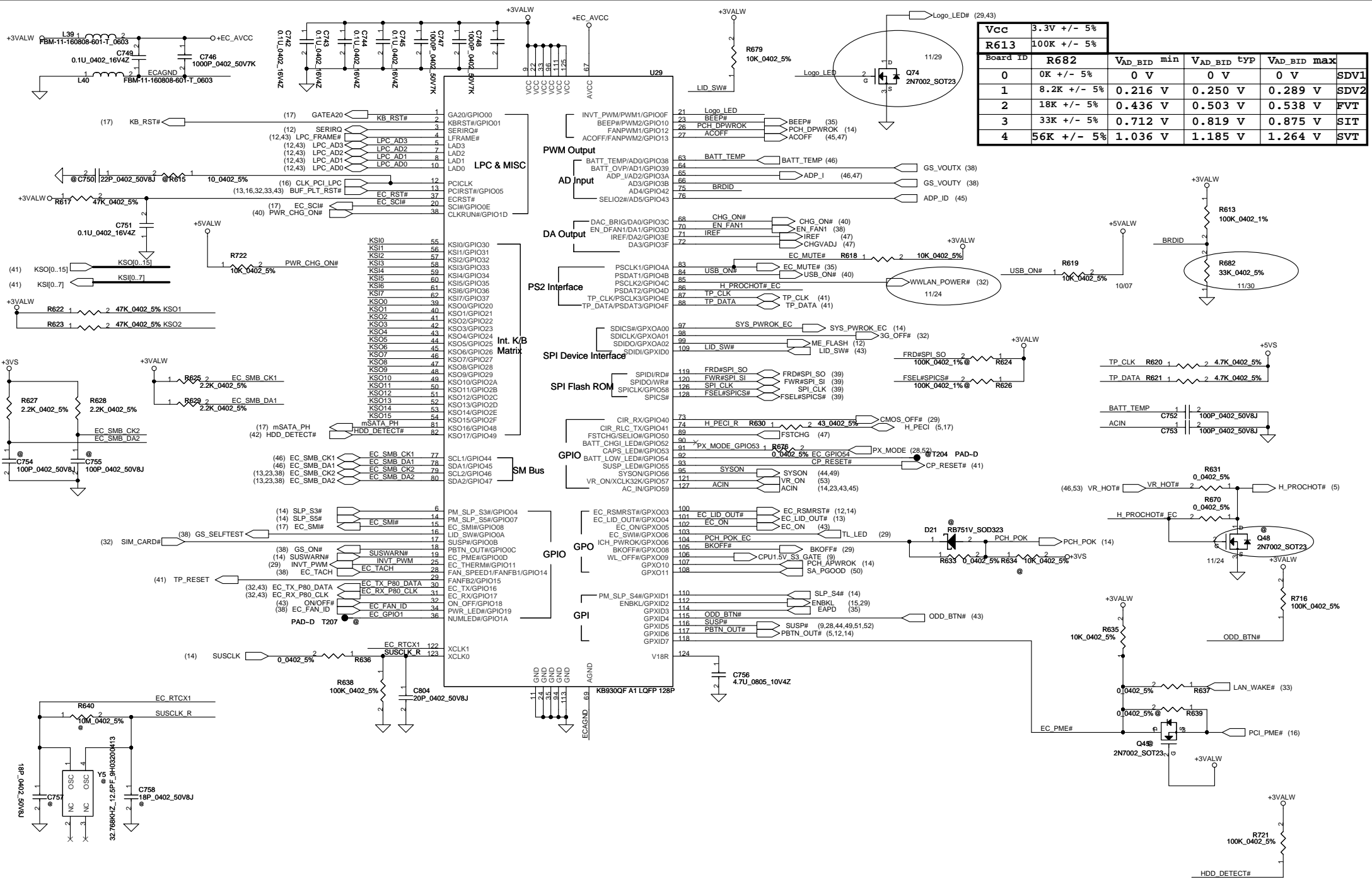
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Choose normal-open type!

Ref Apple  
7:MIC  
5:GND  
4:L  
3:normal close  
1:R  
2:Detect  
6:Normal open

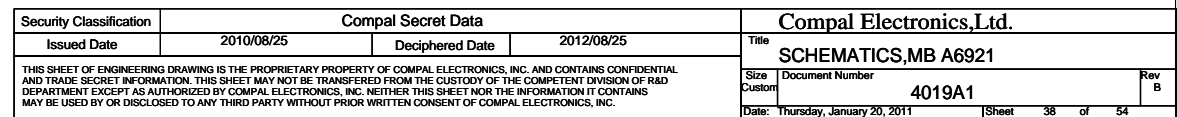
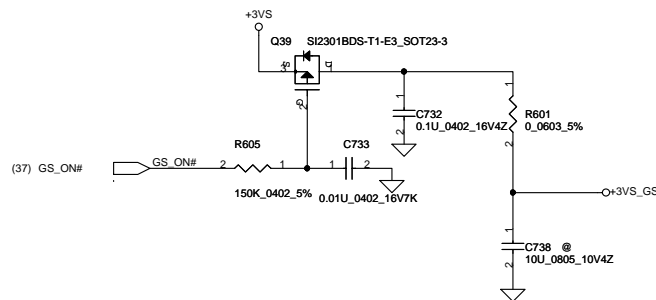
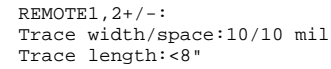
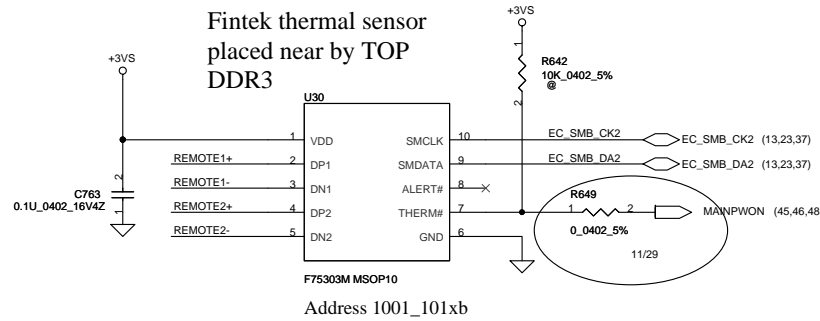


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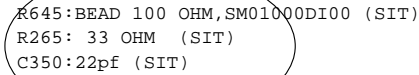
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Document Number				4019A1				Rev			
Date: Thursday, January 20, 2011				Sheet				37 of 54			



FOR EC 128KB SPI ROM  
(150mil PACKAGE)  
PN:SA00002C100



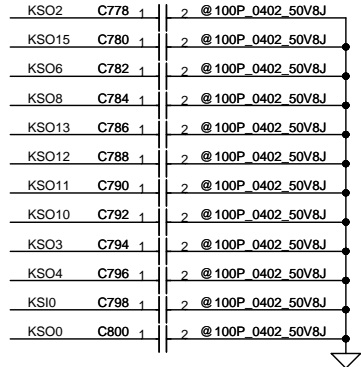
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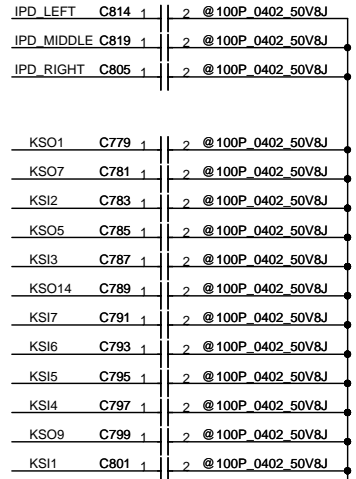


# INT\_KBD Conn.

KSII[0..7] (37)  
KSO[0..15] (37)



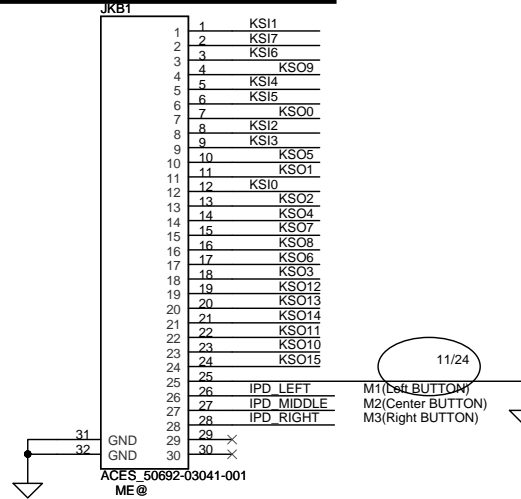
CONN PIN define need double check



Reserve for ESD.

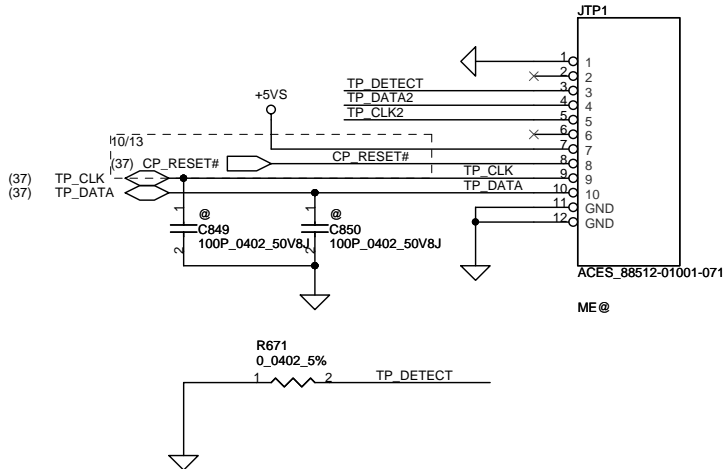
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9/8



PN:LTCX002RM00

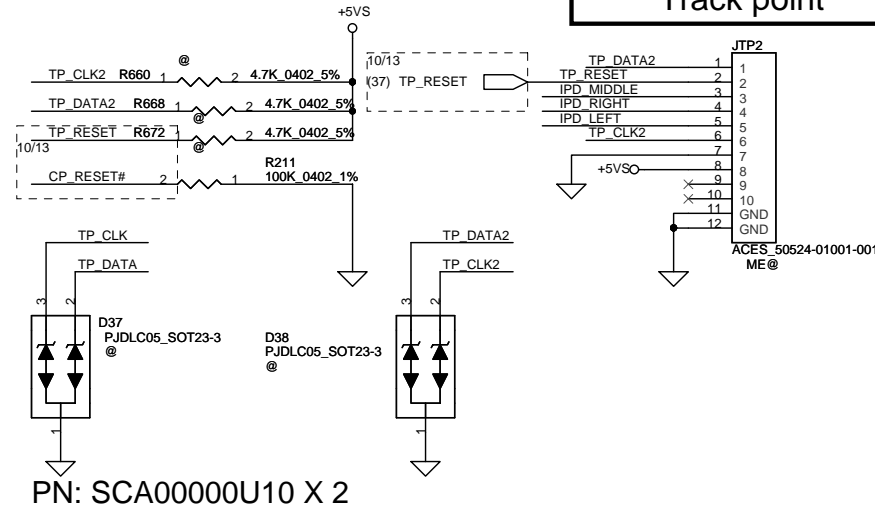
Click pad 10PIN



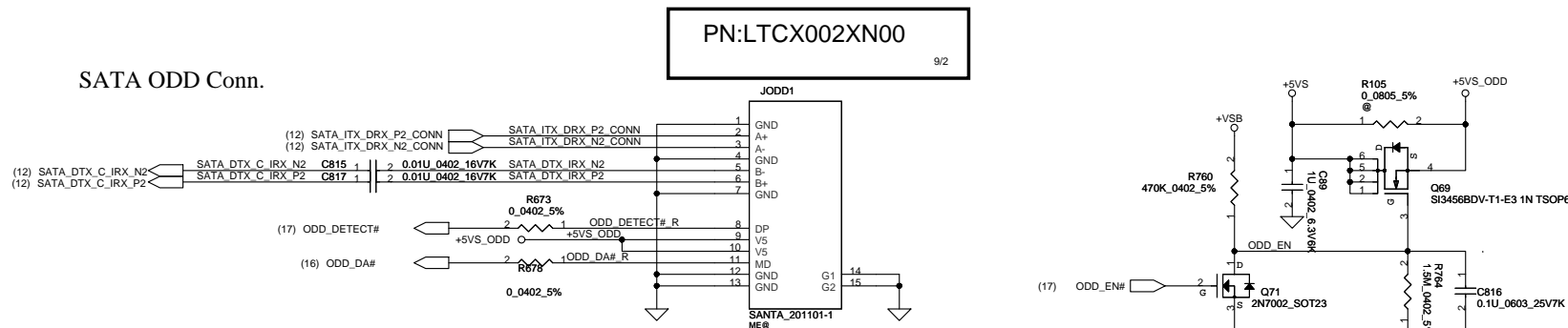
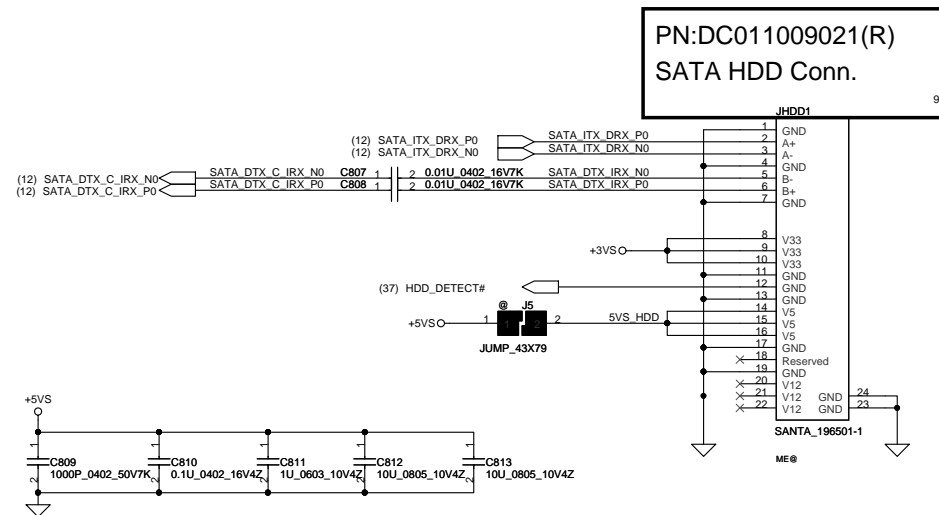
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Track point

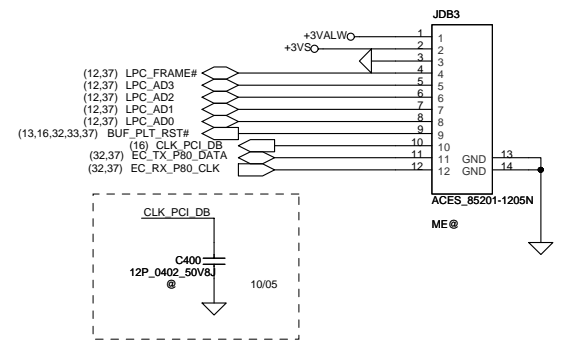
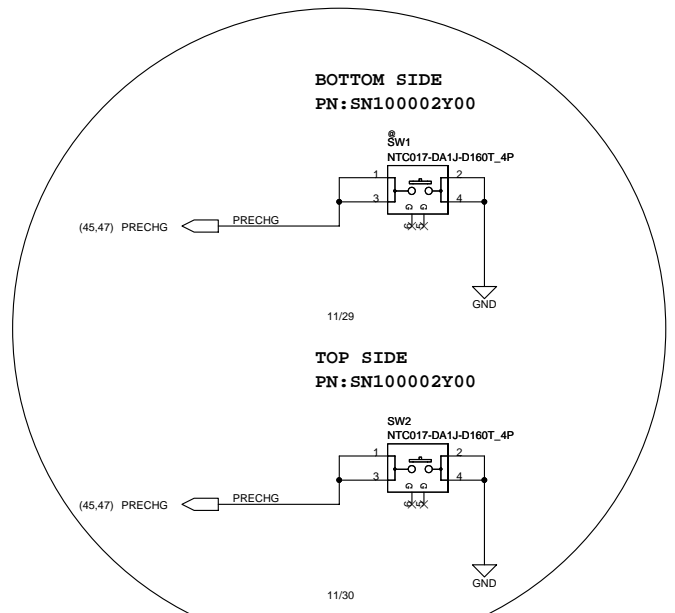
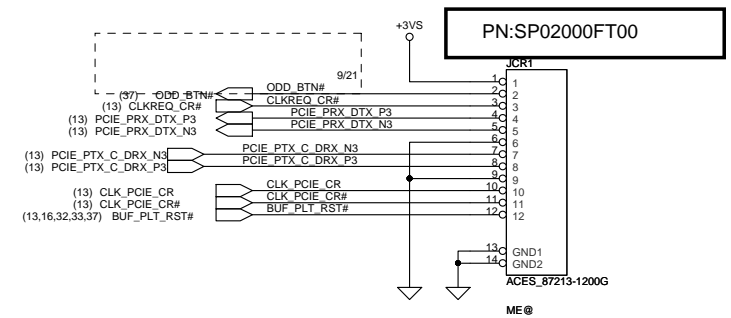
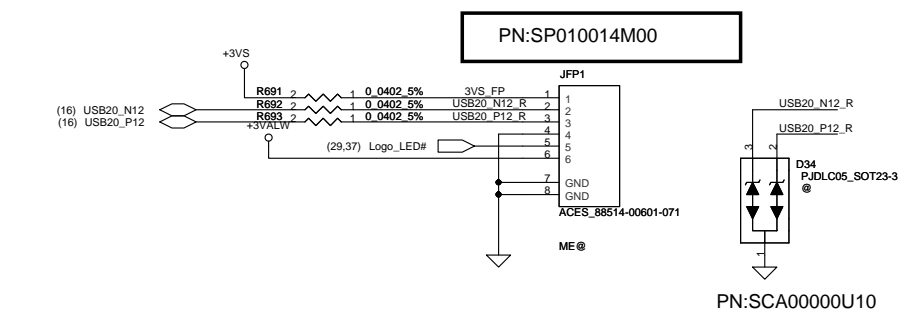
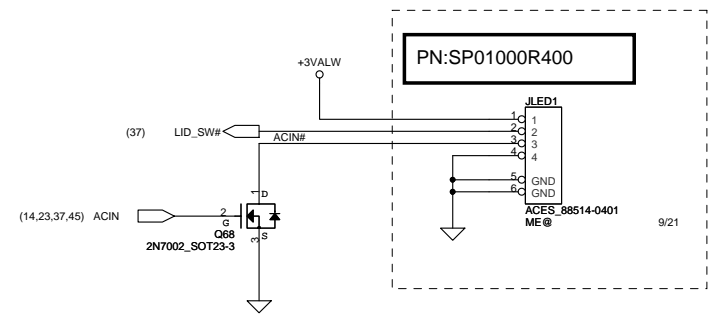
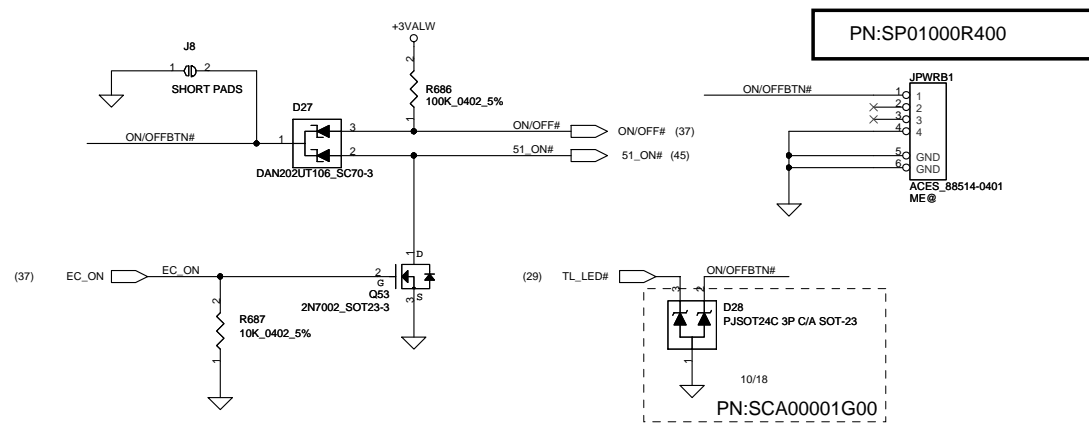
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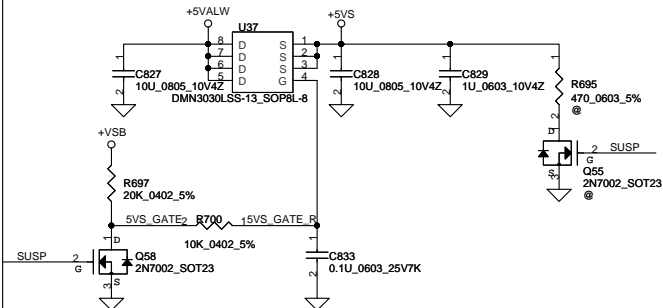


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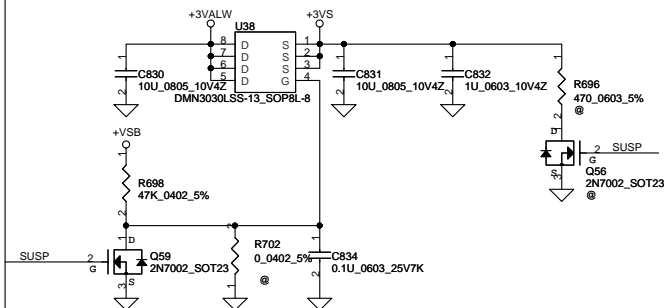


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				Custor	4019A1	B
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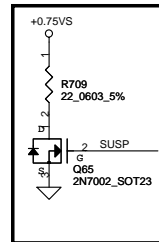
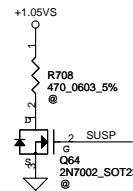
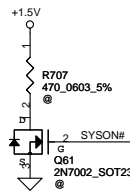
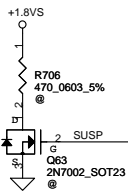
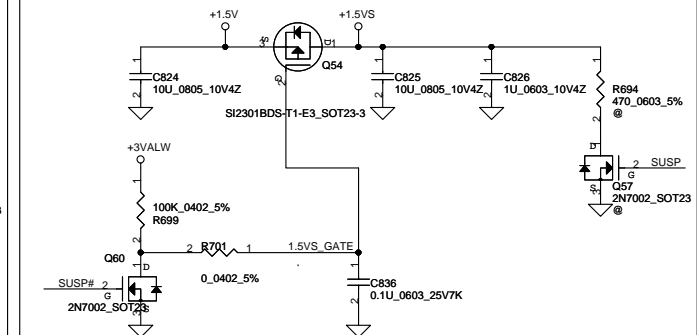
+5VALW TO +5VS



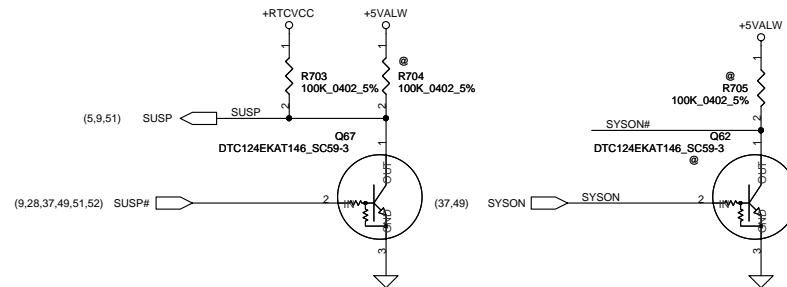
+3VALW TO +3VS



+1.5V to +1.5VS

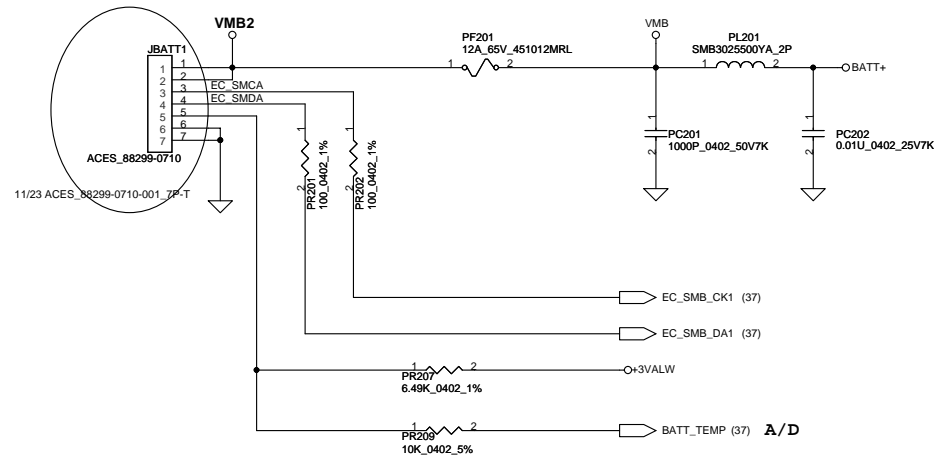


For Intel S3 Power Reduction.

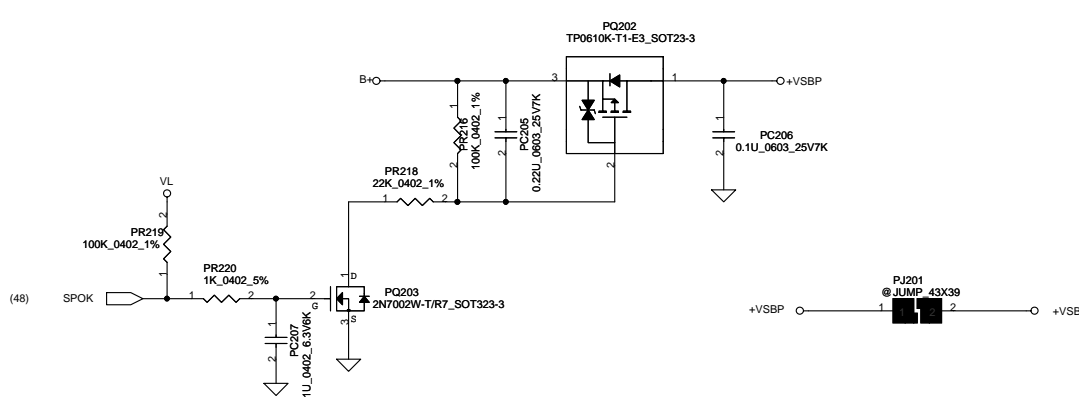
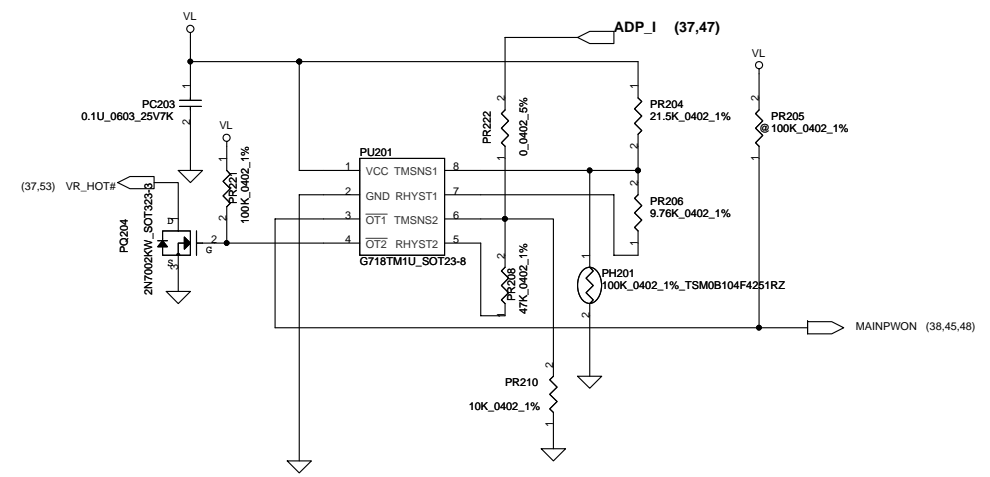


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PH201 under CPU botten side :  
CPU thermal protection at 92 degree C  
Recovery at 56 degree C

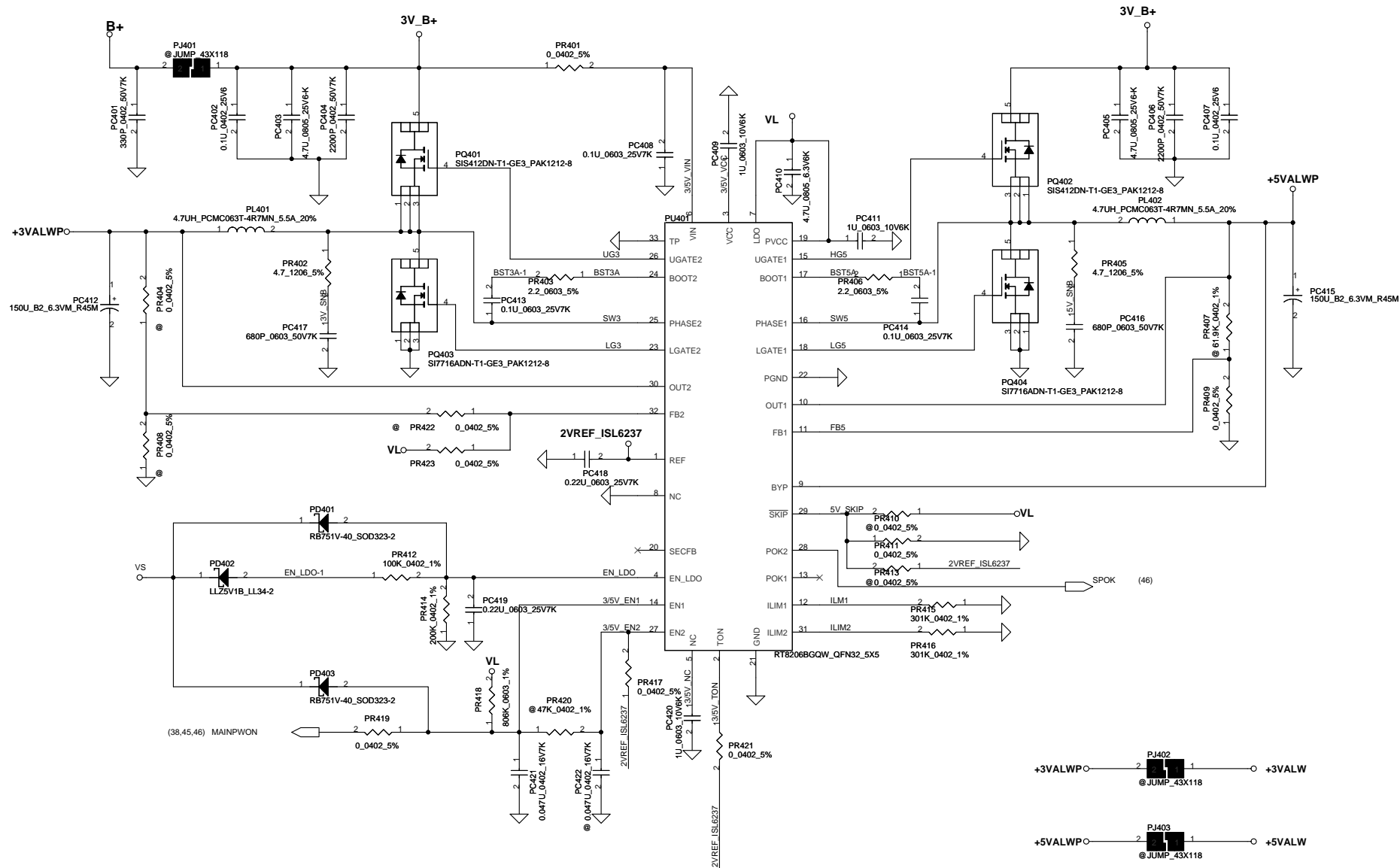


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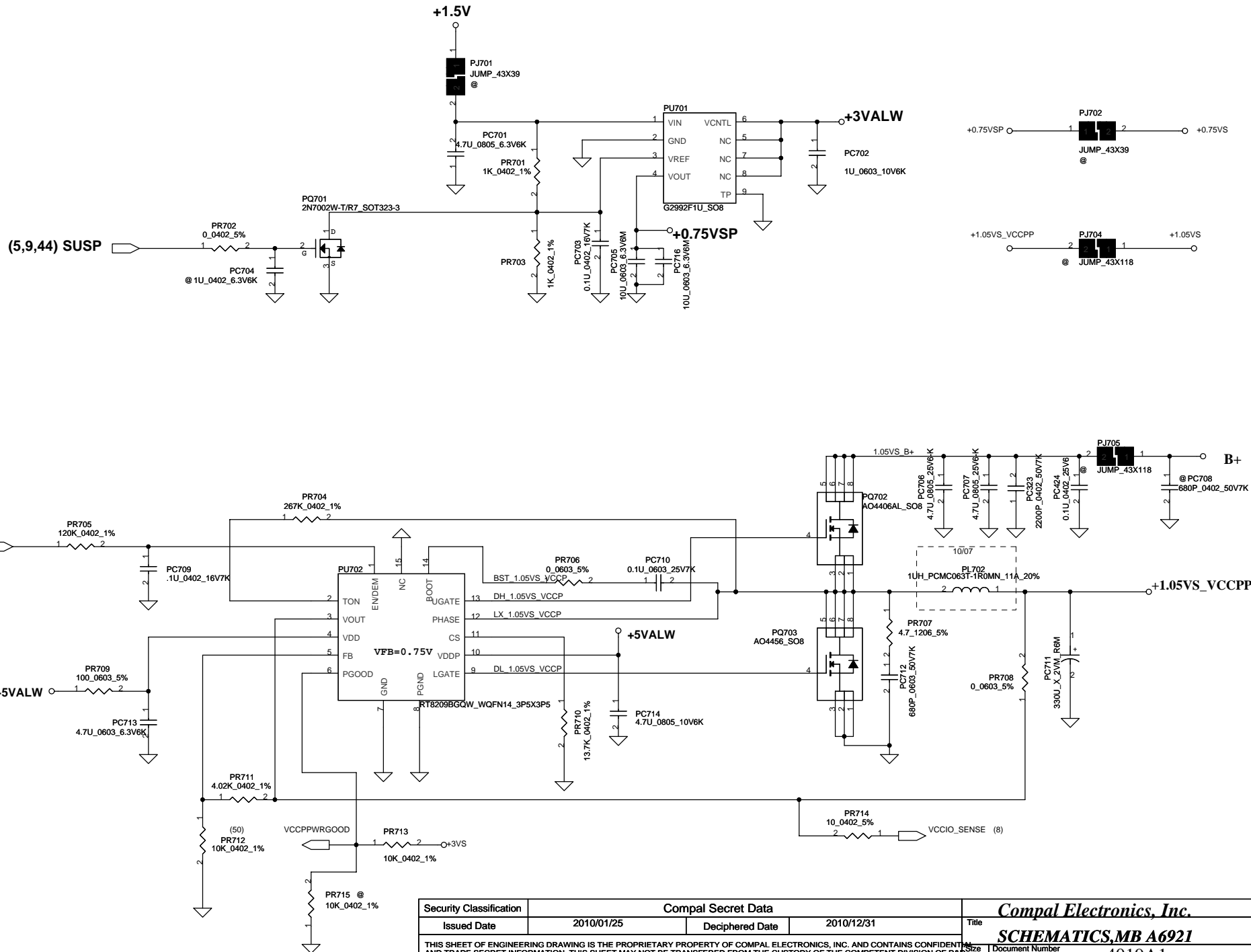
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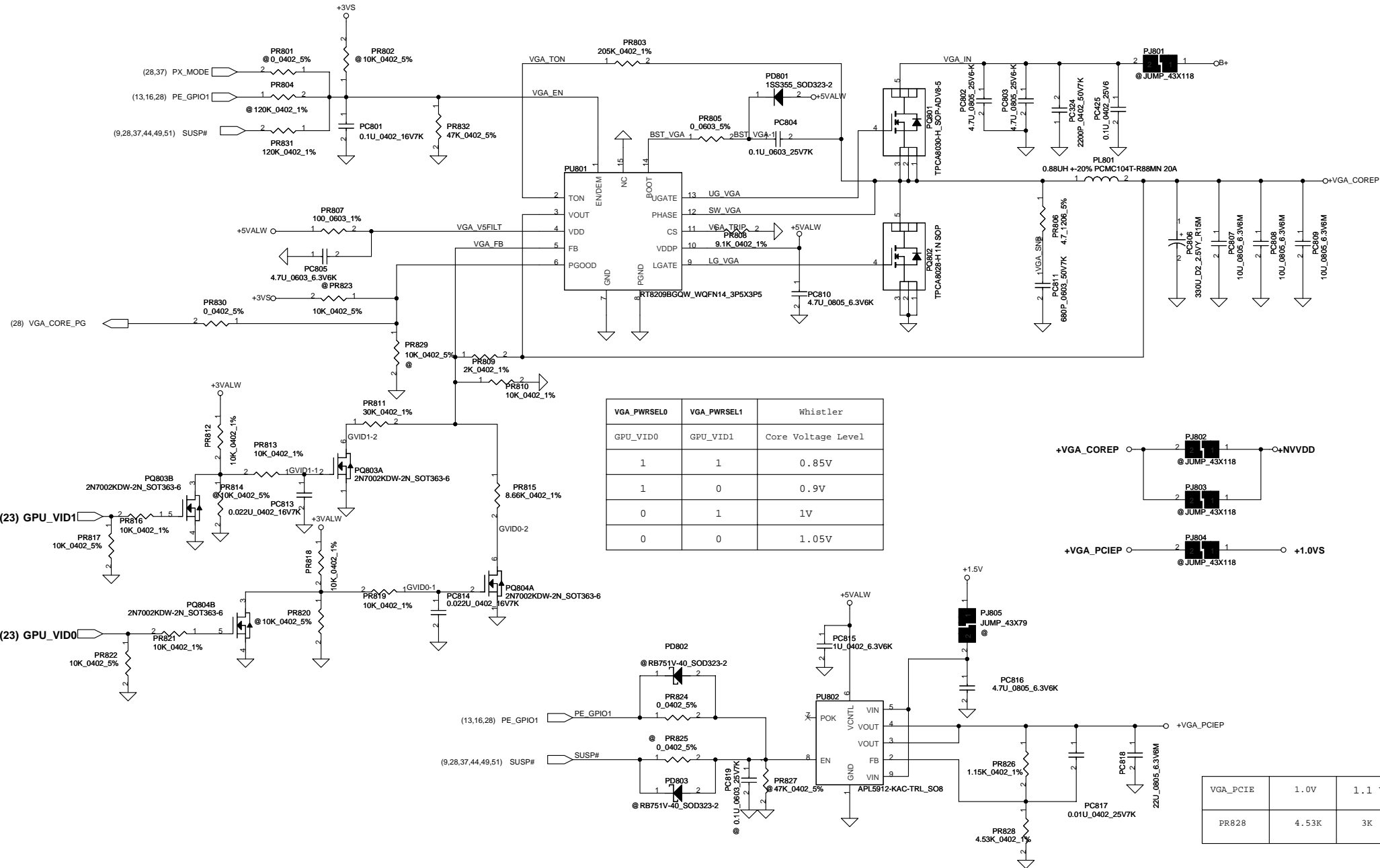


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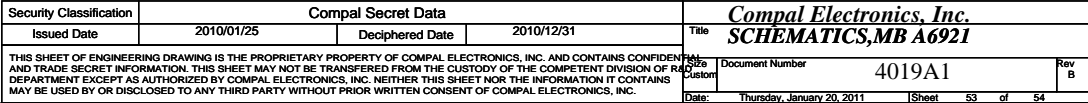








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Item	Reason for change	PG#	Modify List	Date	Phase
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